

UAPC-1100 General Purpose Input/Output (GPIO)

Features

- ◆ Compliance with the AMBA™ Spec. 2.0
- ◆ Individually programmable input/output pins
- ◆ Scalability of data width and masking operation
- ◆ Programmable interrupt generation capability
- ◆ Hardware control capability of GPIO lines
- ◆ Bit masking in both read and write operations through address lines or mask registers

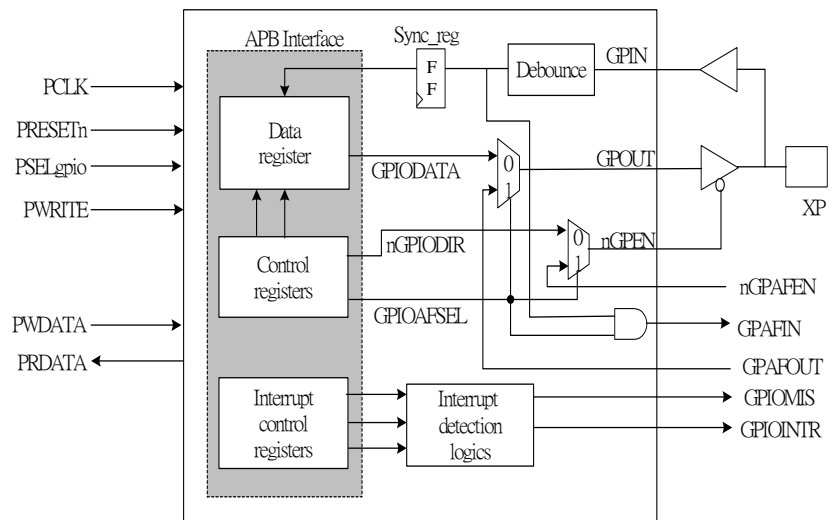
Overview

The UAPC-1100 is a synthesizable soft IP core connected to AMBA™ APB bus for easy integration into SOC implementations.

It provides 8, 16, or 32 programmable input/output ports. The direction of ports can be individually controlled as input or output. Moreover, the GPIO ports can be accessed through APB bus interface or through a hardware control interface.

This module also incorporates interrupt detection capability to generate interrupts. It can be configured to detect interrupts depending on a level, or a transitional value of input pins.

Block Diagram



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Description

The UAPC-1100 is an AMBA™ compliant SOC peripheral. It is a slave module that connects to the Advanced Peripheral Bus (APB). The GPIO interfaces with input and output pad cells using a data Input, data output, and output enable per pad.

It provides 8, 16, or 32 programmable I/O ports that can be individually configured to software control mode or hardware control mode. The GPIO port is accessed through APB bus interface in software control mode. In hardware control mode, the GPIO port is accessed by external control block through hardware control interface.

An interrupt interface is provided to configure any number of pins as interrupt source. It can generate interrupts depending on a level, or transitional value of pins by programming a set of interrupts configuration registers.

Deliverables

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set including Datasheet, User Manual, Verification Guide, and Test Guide

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