

UAPC-1400 Real-Time Clock

Features

- ◆ Compliance with the AMBA™ Spec. 2.0
- ◆ Separated second, minute, hour, and day counters to reduce power consumption and software complexity
- ◆ Programmable auto every second, minute or hour alarm AHB burst transfers

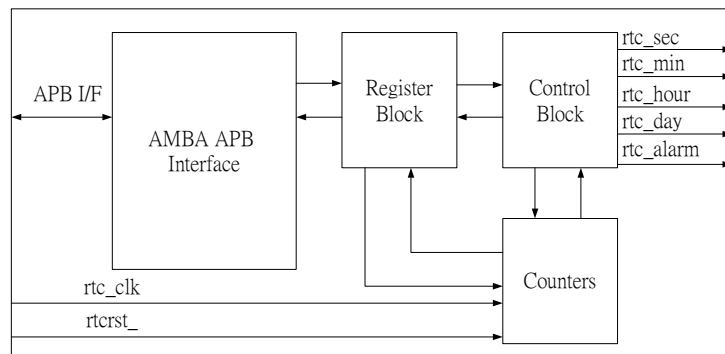
Overview

The UAPC-1400 *Real-Time Clock* (RTC) is an *Advanced Microcontroller Bus Architecture* (AMBA) compliant System-on-Chip (SOC) peripheral that is developed, tested and licensed by GUC.

The GUC RTC is an AMBA slave module that connects to the *Advanced Peripheral Bus* (APB).

The GUC RTC can be used to provide a basic alarm function or counters. This is achieved by generating interrupt signals after counting for a programmed number of cycles of a real time clock input. Counting in one-second intervals is achieved by use of a 1Hz clock input to GUC RTC.

Block Diagram



Description

GUC RTC comprises:

- An AMBA APB interface.
- Dedicated second, minute, hour, and day counter
- Programmable second, minutes, hour, and day match register

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The CPU reads and writes data and control/status information via the AMBA APB interface.

The second counter is incremented on successive rising edges of the input clock CLK1HZ. Counting in one-second intervals is achieved by using 1Hz clock signal for CLK1HZ. The second, minute, hour, and day counters are loaded with a start value by writing to the load register. The value of the counters may be obtained at any time by reading the data register. When the counters reach the max, it wraps to zero and continues incrementing.

The match register is programmed by write match register. The counter and match values are compared in a comparator. When both values are equal, the interrupt signals are asserted HIGH. The CPU can use the interrupt to implement a basic time alarm function. The value in the match register may be read at any time.

Writing to the interrupt control register can mask the interrupt signals. The status of the interrupt may be obtained by reading status register.

Deliverables

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set including Datasheet, User Manual, Verification Guide, and Test Guide

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