

## UAPC-2100 Digital Audio Interface Receiver

### Features

- ◆ Compliance with the AMBA Specification 2.0
- ◆ Support multiple digital audio interfaces formats
- ◆ Support I<sup>2</sup>S, MSB extended, Left-justified, Right-justified data format
- ◆ Software programmable word length, support 1 to 24 valid bits/word
- ◆ Software programmable word ignored bits, support 0~31 bits
- ◆ Support 1~24 bits/word packet mode
- ◆ Software programmable reset signal
- ◆ Software programmable enable bit
- ◆ Software programmable data received order
- ◆ Provide data sampling on rising or falling edge of serial clock
- ◆ Support for Direct Memory Access (DMA)

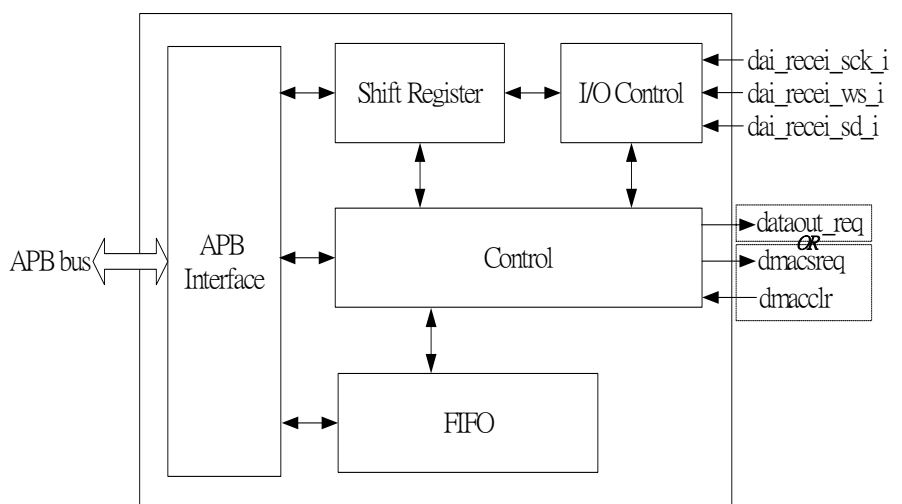
### Overview

The DAI (Digital Audio Interface) receiver provides receiving function of digital audio interface. It can be programmed for supporting multiple data transfer formats, such as I<sup>2</sup>S, MSB extended, Left-justified and Right-justified data format. The received data is stored into an internal FIFO. The dmaclsreq / dataout\_req signal sends request for DMA/CPU to removing data from the FIFO to a storage device.

The DAI receiver can be reset by software programmable reset to bring DAI receiver into reset status.

The DAI Receiver is a synthesizable soft IP core that connects to AMBA™ APB bus for easy integration into SOC implementation. Resulting from a disciplined IP authoring process and going through a functional verification, this core is extremely robust. Its full-scan feature boosts the fault coverage to over 99%.

### Block Diagram



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## Description

The DAI receiver is an AMBA compliant SOC peripheral. It is a slave module when connected to an AMBA system.

The transfer format can be decided by setting the configuration registers through APB interface. The digital audio data interface connects with ADC or DAI transmitter by three lines: sck - serial clock, sd - serial data, ws – word select. After the received data has been written into its local FIFO, the DAI receiver will send the data output request signal to DMA (dmacsreq) or CPU (dataout\_req) for removing data to a storage device. The DMA will send the dmaccr (DMA request acknowledge clear) signal back to DAI receiver to clear the dmacsreq signal.

There are six memory-mapped registers accessible through APB interface. Setting the dai\_recei\_sw\_reset register can bring the DAI receiver to the reset state. The dai\_recei\_enable register enables or disables the DAI receiver function. The dai\_recei\_ctrl, dai\_recei\_wlen and dai\_recei\_wpos registers decide the serial interface signals polarity and received data format. The received data is stored into the dai\_recei\_data register implemented as an FIFO.

## Deliverables

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set including Datasheet, User's Manual, Integration Guide, Verification Guide, and Test Guide

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