

## UDAC-2008-250EF

### 0.25 $\mu$ m EmFlash 2.5V/3.3V 8-bit 500Ksps DAC [2ch]

#### Features

- ◆ 0.25 $\mu$ m 2.5V/3.3V Mixed-Signal salicide CMOS process with 1P4M layout
- ◆ 3.3V for analog core and 2.5V for digital core
- ◆ Output voltage range: 0~2.0V
- ◆ Typical output current: 1mA at full scale (single-ended)
- ◆ Monotonic guaranteed
- ◆ Generic DAC with 2 channels
- ◆ Operation temperature range: 0 $^{\circ}$ C~75 $^{\circ}$ C
- ◆ Build-in voltage reference
- ◆ Power down mode available
- ◆ Test chip available in LQFP-48 package

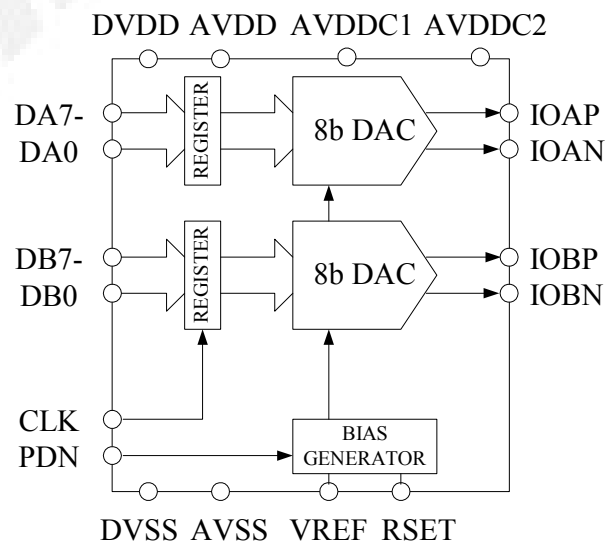
#### Applications

- Portable Battery Powered Application
- Mass storage device
- Instrumentation

#### Overview

UDAC-2008-250EF is a general purpose digital to analog converter (DAC). The DAC is implemented using current steering; therefore the produced output current is proportional to the input code. A power down mode is available with this IP core.

#### Block Diagram



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## Description

The UDAC-2008-250EF is a dual-channel, digital to analog converter macro with 8-bit resolution. The DAC receives the digital input code and convert them to the corresponding output current. The  $I_{LSB}$  (Least Significant Bit current) has a ratio of 0.1 to the current determined by the setting resistor connecting between RSET to AVSS and the build-in reference voltage, VREF. The equivalent is given by:

$$IOxP = \frac{VREF}{RSET} \times (\text{Digital input code}) \times 0.1$$

$$IOxN = \frac{VREF}{RSET} \times (255 - \text{Digital input code}) \times 0.1$$

$$\text{Digital input code} = Dx_7 \cdot 2^7 + Dx_6 \cdot 2^6 + Dx_5 \cdot 2^5 + Dx_4 \cdot 2^4 + Dx_3 \cdot 2^3 + Dx_2 \cdot 2^2 + Dx_1 \cdot 2^1 + Dx_0 \cdot 2^0$$

## Deliverables

- Comprehensive document set
- Hard macro
- Synopsys™ synthesis model
- Verilog model
- TLF model
- LEF model
- Testchip and evaluation board

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