

ULVR-3318C-180

0.18 μ m 3.3V to 1.8V/1.5V/1.2V 150mA Linear Voltage Regulator

Features

- ◆ 0.18 μ m 1.8V/3.3V logic salicide CMOS process with 1P4M layout
- ◆ 3.3V to 1.8V/1.5V/1.2V
- ◆ Programmable output voltage
- ◆ Low drop-out voltage
- ◆ Maximum output load current: 150mA
- ◆ Operation temperature range: 0 $^{\circ}$ C~75 $^{\circ}$ C
- ◆ Build-in voltage reference
- ◆ Power down mode available
- ◆ Stable with 1 μ F ceramic capacitor
- ◆ Test chip available in LQFP-64 package
- ◆ Customized I/O pads available

Applications

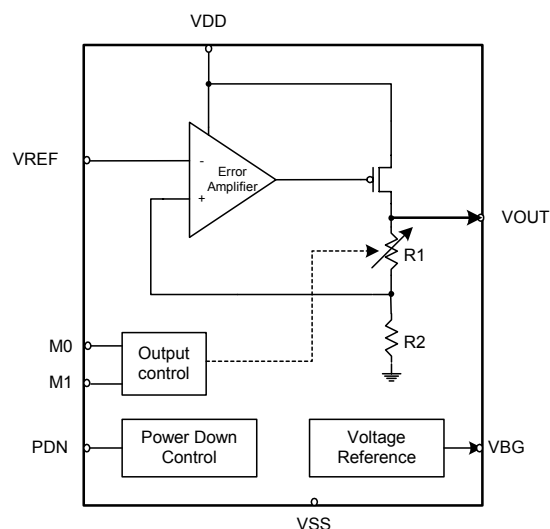
- PCMCIA Card
- Camera
- Battery Powered Application

Overview

ULVR-3318C-180 is a linear voltage regulator (LVR) IP for powering the 1.8/1.5V/1.2V digital core circuit from single 3.3V supply voltage. It provides an operating voltage of 1.62V~3.63V. The regulator incorporates a bandgap circuit for fixing reference voltage generation. The feedback loop sets the output voltage to 1.8V/1.5V/1.2V with small voltage coefficient regardless whether the output load current changes from 0mA up to 150mA or supply voltage varies.

A bypass capacitor is required for proper frequency compensation. A power down mode is available for the regulator.

Block Diagram



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Description

The output voltage of the regulator (V_{OUT}) is set by the V_{REF} and the output voltage control signal M_0 and M_1 . By setting M_0 and M_1 digital control signal to program the output voltage to 1.8V/1.5V/1.2V. The relationship between the regulator output V_{OUT} and input reference voltage V_{REF} is defined as:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2} \right), \quad 1.12V \leq V_{REF} \leq 1.30V$$

The output voltage will be 1.8V by setting both M_0 and M_1 to logic "0".

The output voltage will be 1.5V by setting $M_0="1"$, $M_1="0"$ or $M_0="0"$, $M_1="1"$.

The output voltage will be 1.2V by setting both M_0 and M_1 to logic "1".

Deliverables

- Comprehensive document set
- Hard macro
- Synopsys™ synthesis model
- Verilog model
- TLF model
- LEF model
- Testchip and evaluation board

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