

UPLL-0006-250

0.25um PLL-Based Clock Generator

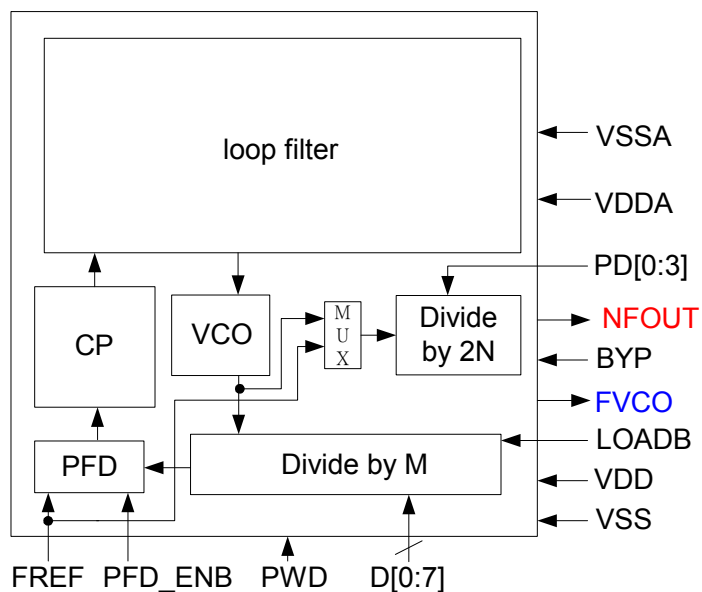
Features

- ◆ 0.25um 1P5M 2.5v/3.3v logic salicide CMOS process with 1P3M layout
- ◆ Separated analog and digital power/ground
- ◆ Fully integrated PLL-based clock generator with built-in loop filter
- ◆ VCO frequency range (100MHz ~ 500MHz)
- ◆ Wide output frequency rang (FOUT: 3.125MHz ~ 250MHz, FVCO: 100MHz~500MHz)
- ◆ Flexible input frequency range (2MHz ~ 60MHz)
- ◆ Two programmable frequency divider (8-bit main divider and 4-bit post divider)
- ◆ Low jitter
- ◆ Bypass mode
- ◆ Power down mode

Overview

The UPLL-0006-250 is a PLL-based clock generator with built-in loop filter. It integrates a voltage-controlled oscillator, a phase frequency detector, a charge pump, a loop filter and two frequency dividers. It can generate frequency range within 3.125MHz~500MHz with an 8-bit main frequency divider and a 4-bit post divider. The UPLL-0006-250 is designed with TSMC 0.25um 1P5M 2.5v/3.3v logic salicide CMOS process.

Block Diagram



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Description

The circuit of UPLL-0006-250 is a PLL designed for clock generation. The output frequency of the PLL can be programmed by the inputs (D[7:0], PD[3:0]). The output frequency of FVCO and FOUT can be controlled by D[7:0] and PD[3:0]. The frequencies are defined as follows:

$$FVCO = FREF * M \quad (M \geq 2, FREF \geq 2Mhz, 500Mhz \geq FVCO \geq 100Mhz)$$

$$FOUT = FREF * M / 2N \quad (M \geq 2, N \geq 1, FREF \geq 2Mhz, 250Mhz \geq FOUT \geq 3.125Mhz)$$

The value of D[7:0] and PD[3:0] is encode with binary weighted code. M is the value of D[7:0]. N is the value of PD[3:0].

Deliverables

- ◆ Comprehensive document set
- ◆ Hard macro
- ◆ Synopsys™ synthesis model
- ◆ Verilog model
- ◆ TLF model
- ◆ LEF model
- ◆ Test chip and evaluation board

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