

## UPOR-3301-250

### 0.25 $\mu$ m 3.3V Power-On-Reset Circuit

#### Features

- ◆ Adjustable High- and Low -Threshold Voltages Ranging from +1.75V to +3.25V in 50mV Increments
- ◆  $\pm 2.5\%$  Accurate Threshold Voltage after Internal Bandgap Voltage Reference Trimming
- ◆ Programmable Reset Timeout Period
- ◆ Resettable via External Control
- ◆ Active-low CMOS Output
- ◆ Open-drain Output with Internal Pull-up Resistor
- ◆ Power Supply Transient Immunity
- ◆ Single Supply 2.25V to 3.63V Operation
- ◆ Low Current Consumption (50 $\mu$ A typ.)

#### Applications

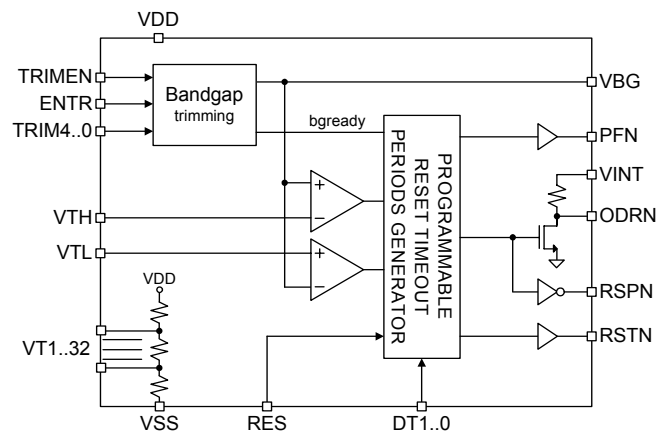
- ◆ Reset of any digital circuitry after power on

#### Overview

The UPOR-3301-250 is a power-on reset circuit (POR) designed with accurate threshold of  $\pm 2.5\%$  (trimmed) or  $\pm 5.6\%$  (untrimmed) variation. The reset timeout periods can be programmed by 2 bits control word ranging from 0.1ms to 100ms.

The UPOR-3301-250 features an additional reset input, which provides another way to generate the reset signal via external control. An open drain output is also available for voltage level conversion.

#### Block Diagram



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## **Description**

The UPOR-3301-250 is a low-power 3.3V power-on reset circuit (POR) designed to monitor the battery voltage in  $\mu$ P and logic systems, and generate a system-reset signal. It provides both configurable reset thresholds and programmable reset timeout periods. In order to make the ODRN output signal compatible to the other core voltage different from 3.3V an open drain output with internal pull-up resistor topology is also provided.

This circuit is implemented in TSMC 0.25  $\mu$ m logic salicide 1P5M 2.5V/3.3V CMOS process with 1P3M layout. The test chip is available in a 64-lead LQFP package. The evaluation board is available with the test chip.

## **Deliverables**

- ◆ **Comprehensive document set**
- ◆ **Hard macro**
- ◆ **Synopsys™ synthesis model**
- ◆ **Verilog model**
- ◆ **TLF model**
- ◆ **LEF model**
- ◆ **Test chip**
- ◆ **Evaluation board**

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